HOOP: Efficient Hardware-Assisted Out-of-Place Update for Non-Volatile Memory

Miao Cai † **Chance Coats** Jian Huang

Systems Platform Research Group

ILLINOIS

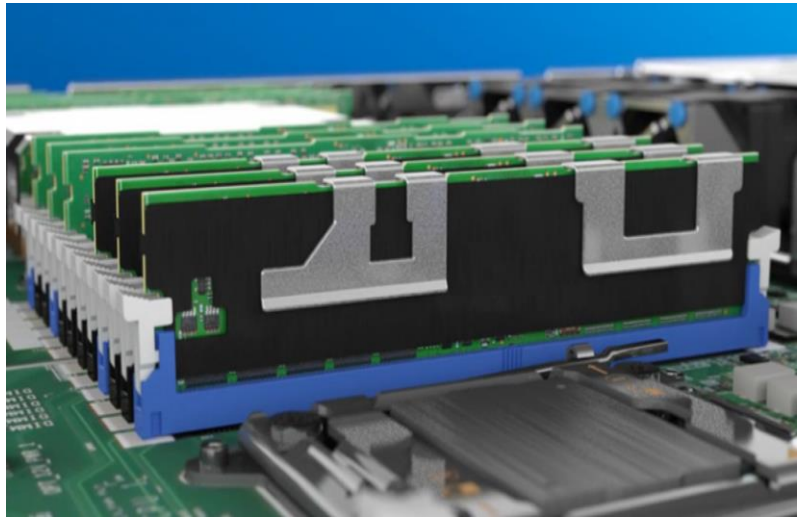
†

NANJING UNIVERSITY 1902

Non-Volatile Memory is a Revolutionary Technology

Close-to-DRAM Performance

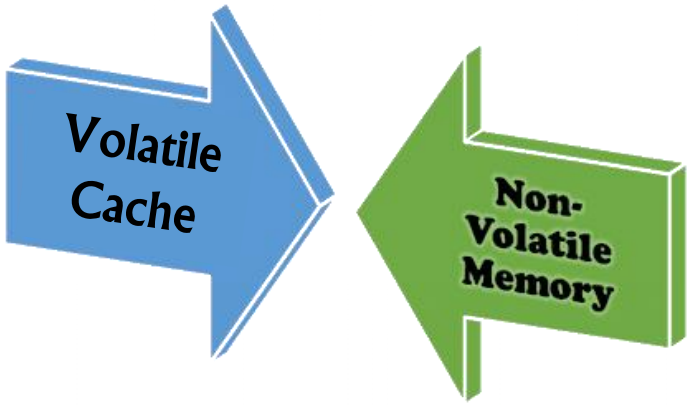
Data Durability



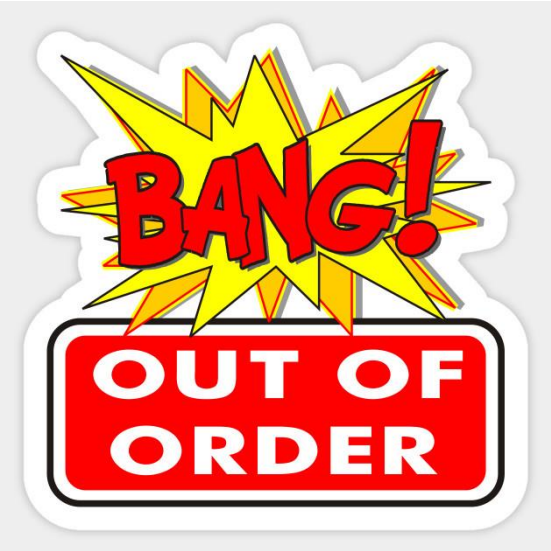
Byte Addressability

New and emerging NVMs offer promising properties and become popular

Memory Persistency Challenge: A Well-Known Problem



Volatile Processor Cache

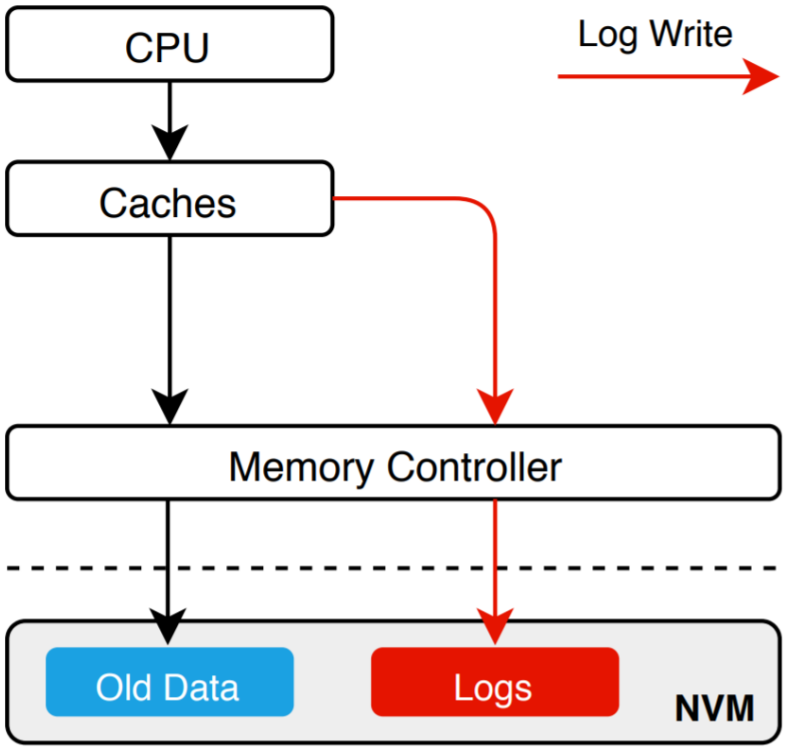


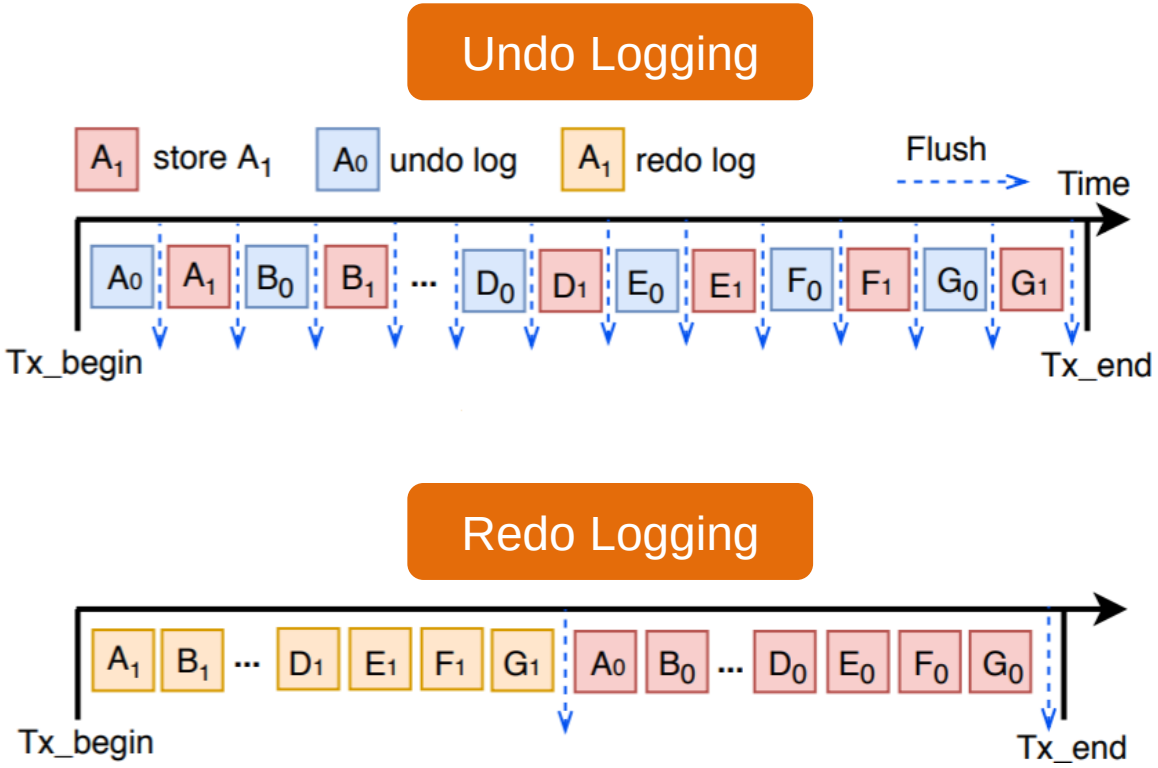
Out-of-Order Execution

Performance vs. Persistency

Ensuring memory persistency with commodity architecture is challenging!

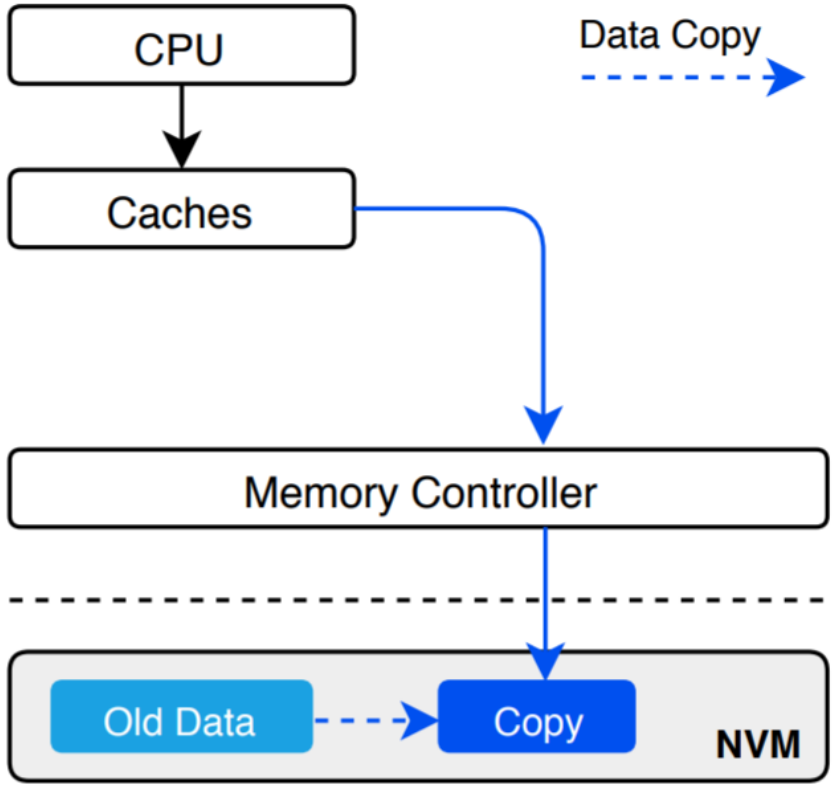
State-of-the-Art Approach: Redo/Undo Logging

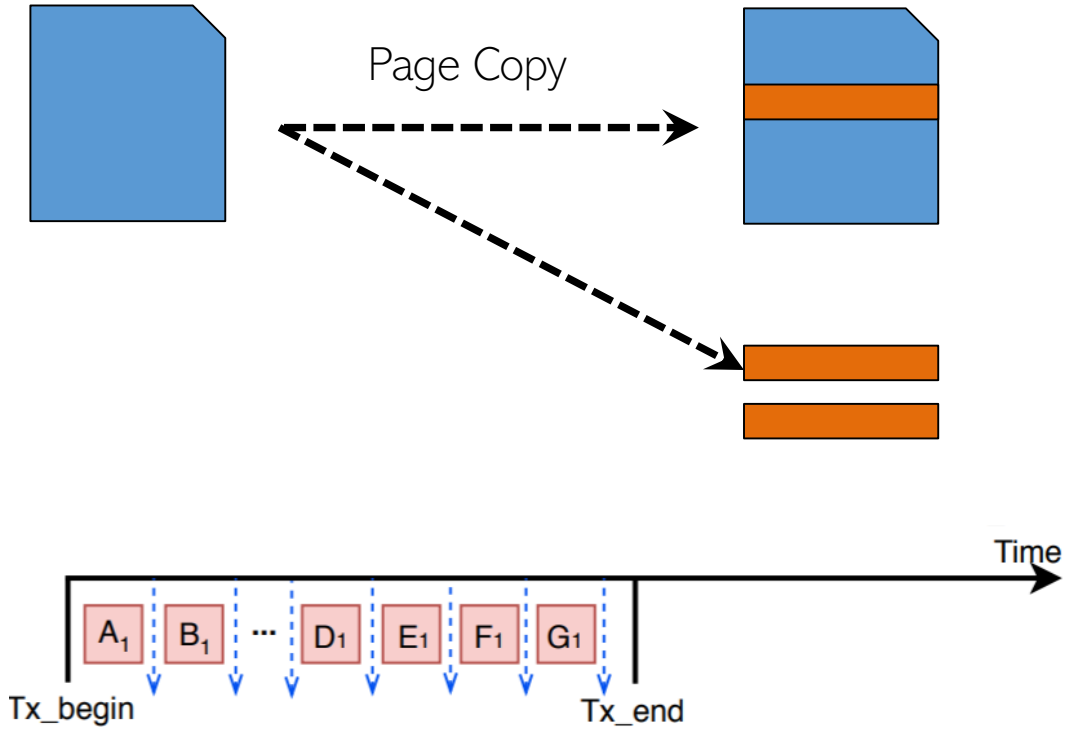




Undo/Redo logging causes **DOUBLE WRITES** on the critical path.

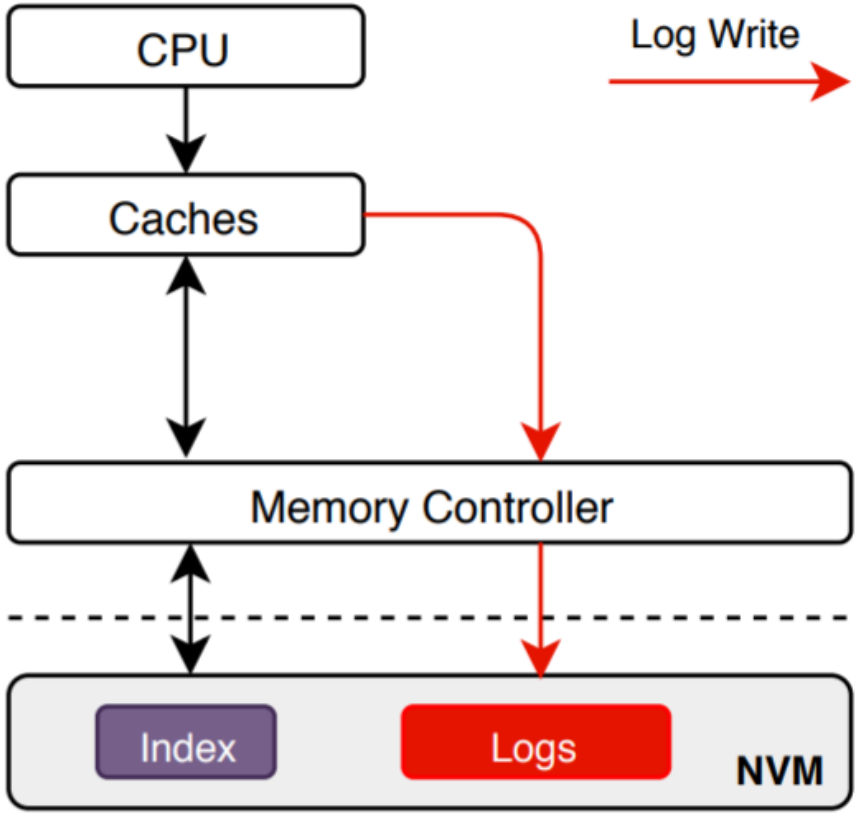
State-of-the-Art Approach: Shadow Paging

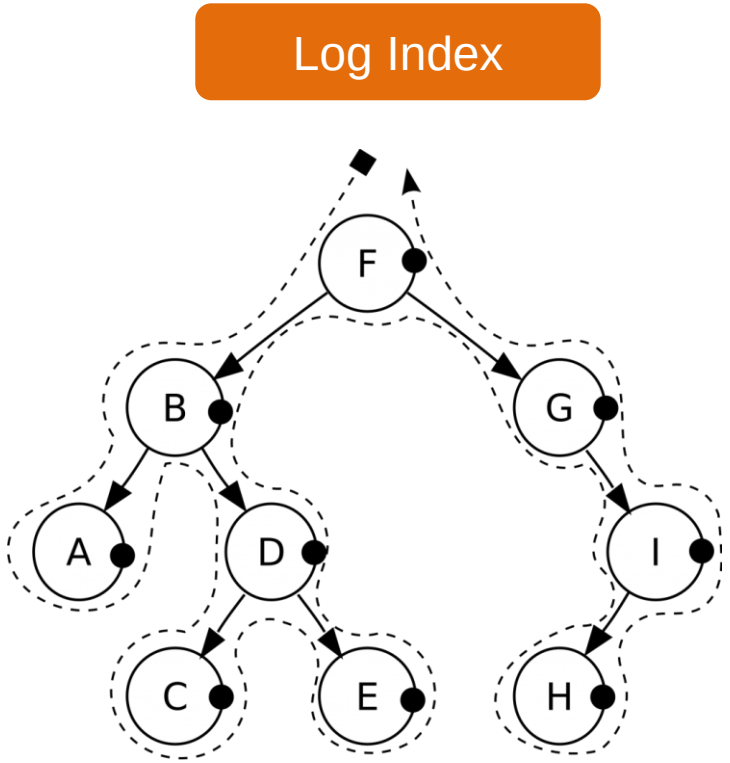




Optimized shadow paging still suffers from **FREQUENT DATA FLUSHES**.

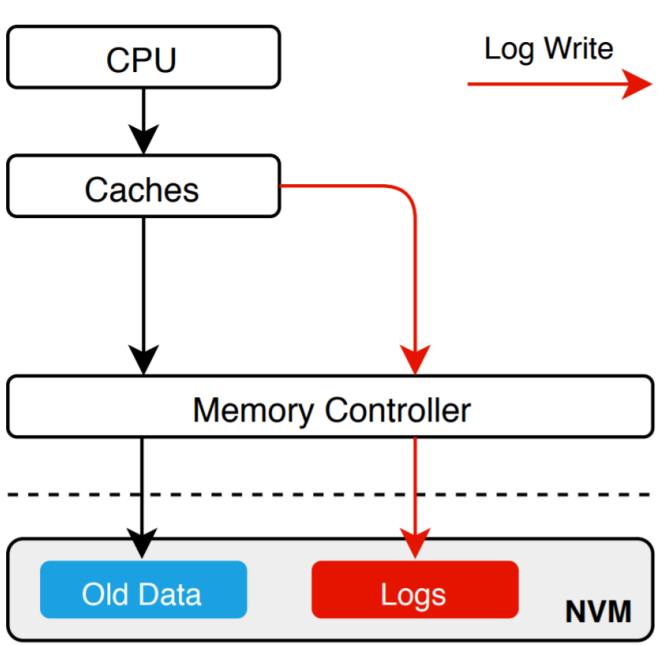
State-of-the-Art Approach: Log-structured NVM



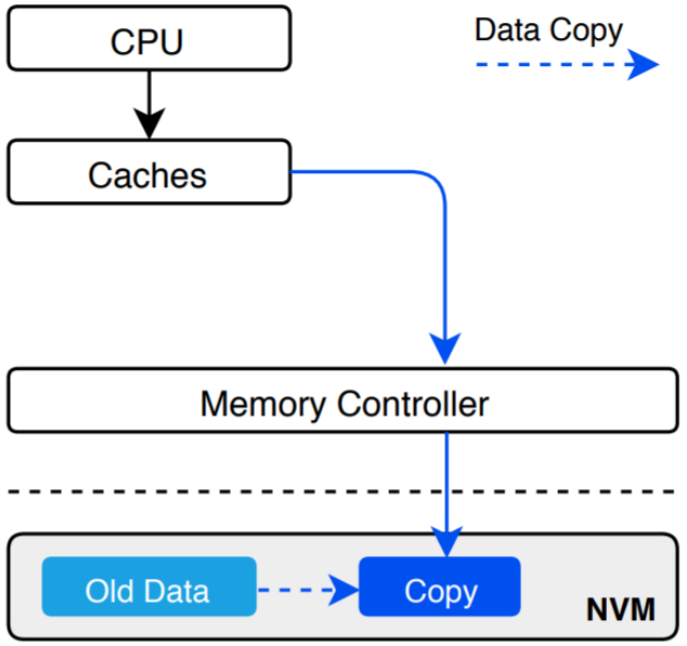


Software-based LSNVM suffers from **LONG ACCESS LATENCY**.

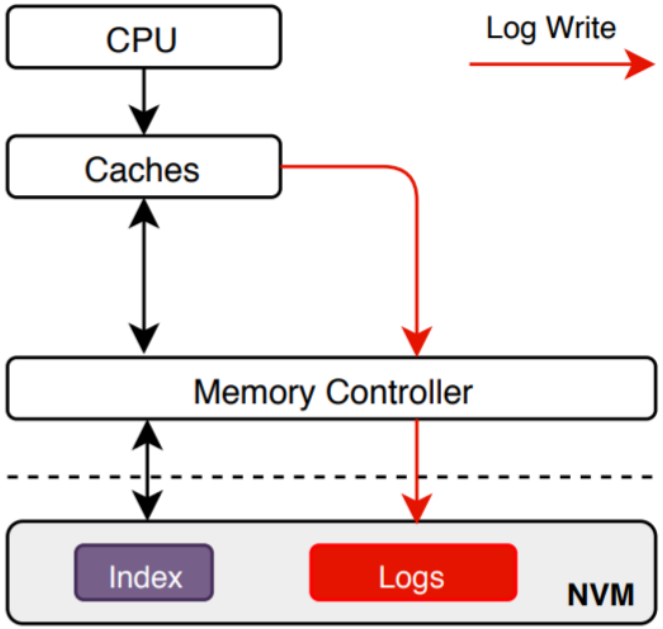
A Summary of State-of-the-Art Approaches



Logging



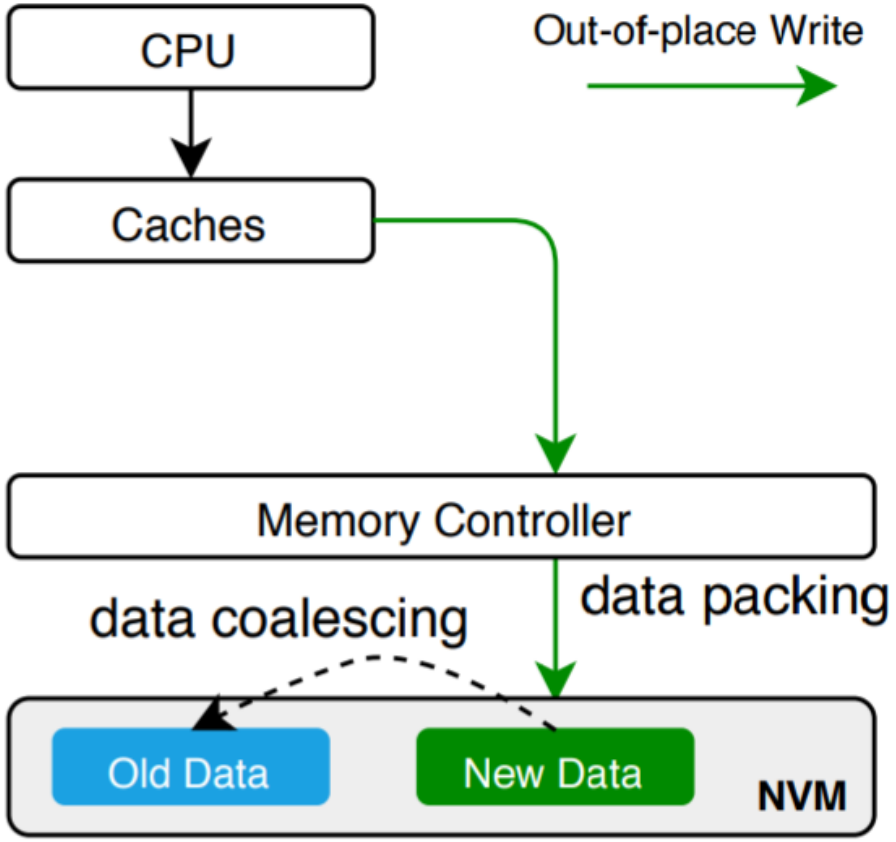
Shadow Paging



Log-structured NVM

Memory persistency overheads: double writes, frequent flushes, long critical-path latency

Our Approach: Hardware-assisted Out-Of-Place (HOOP) Update



Reduced write traffic with data coalescing and packing

+

No requirement on persistence ordering

+

Transparent support of atomic data durability

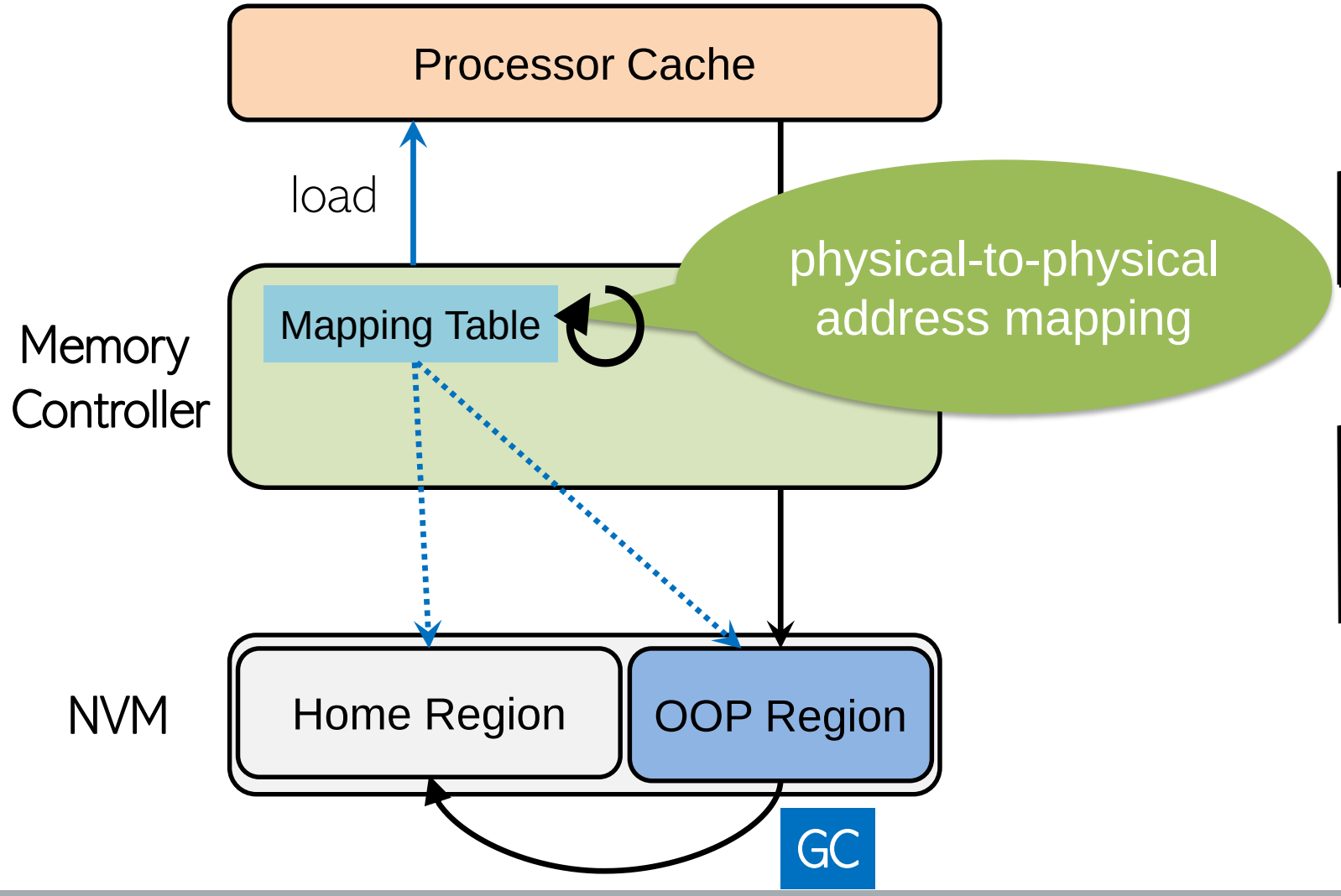
Challenges of Supporting Out-Of-Place Update

Lightweight Indirection Layer

Limited Resource in Memory Controller

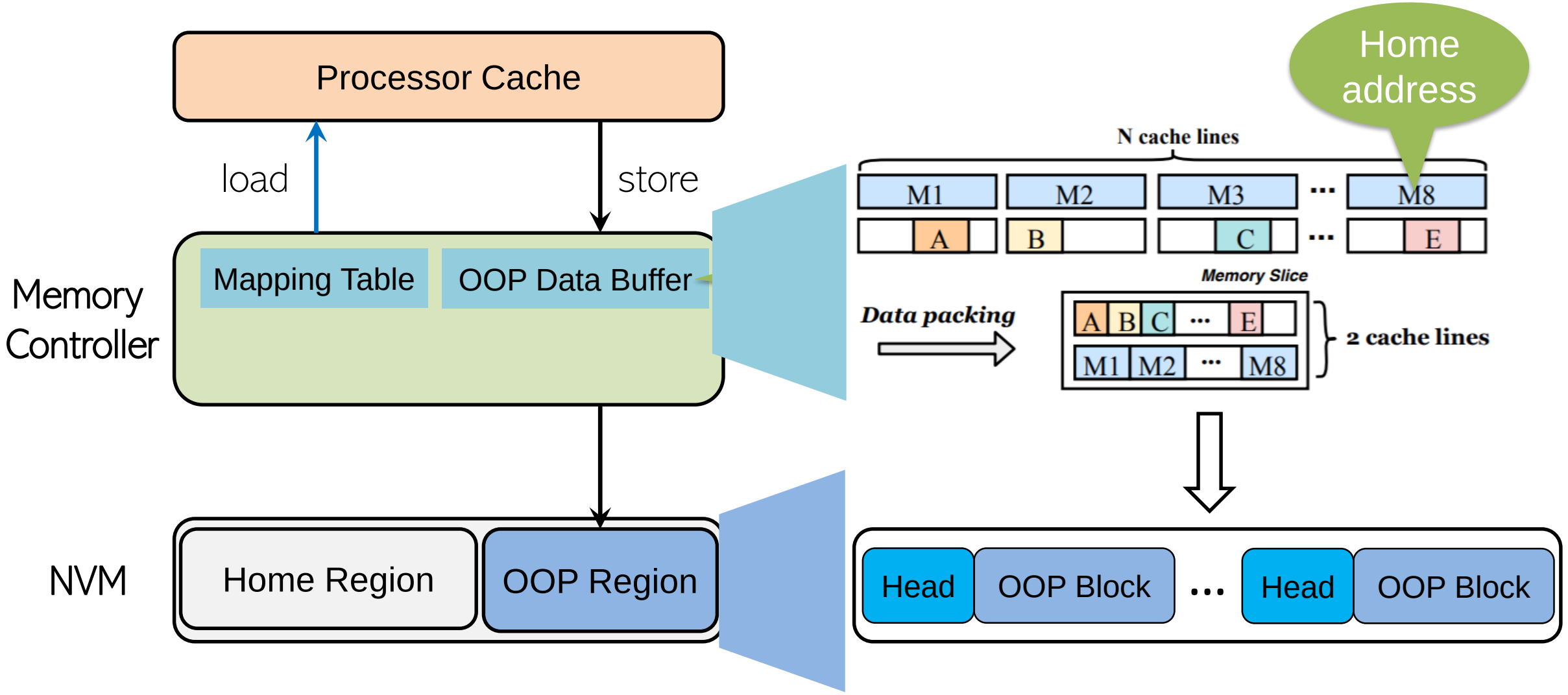
Efficient Garbage Collection

Address Remapping for Supporting Out-of-Place Update

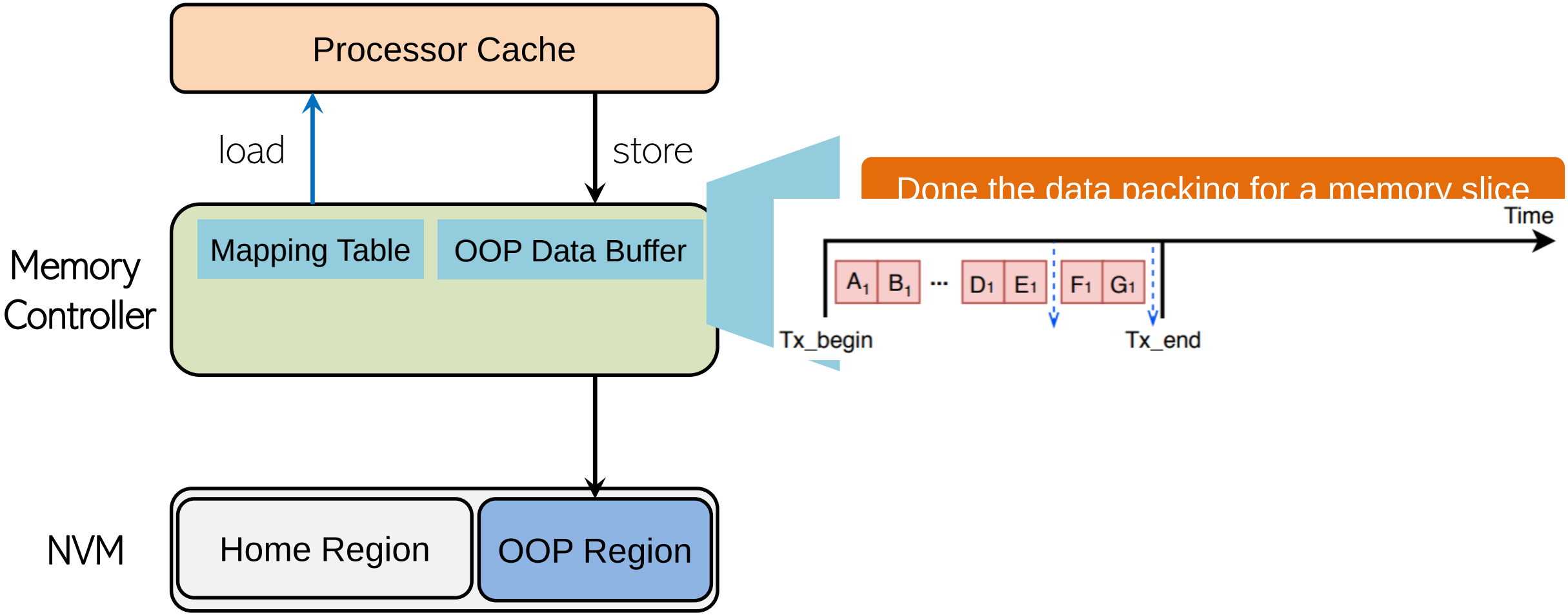


- Insert mapping entry
  - Upon a write to OOP region
- Delete mapping entry
  - Data migration from OOP to home
  - Upon a read from OOP region

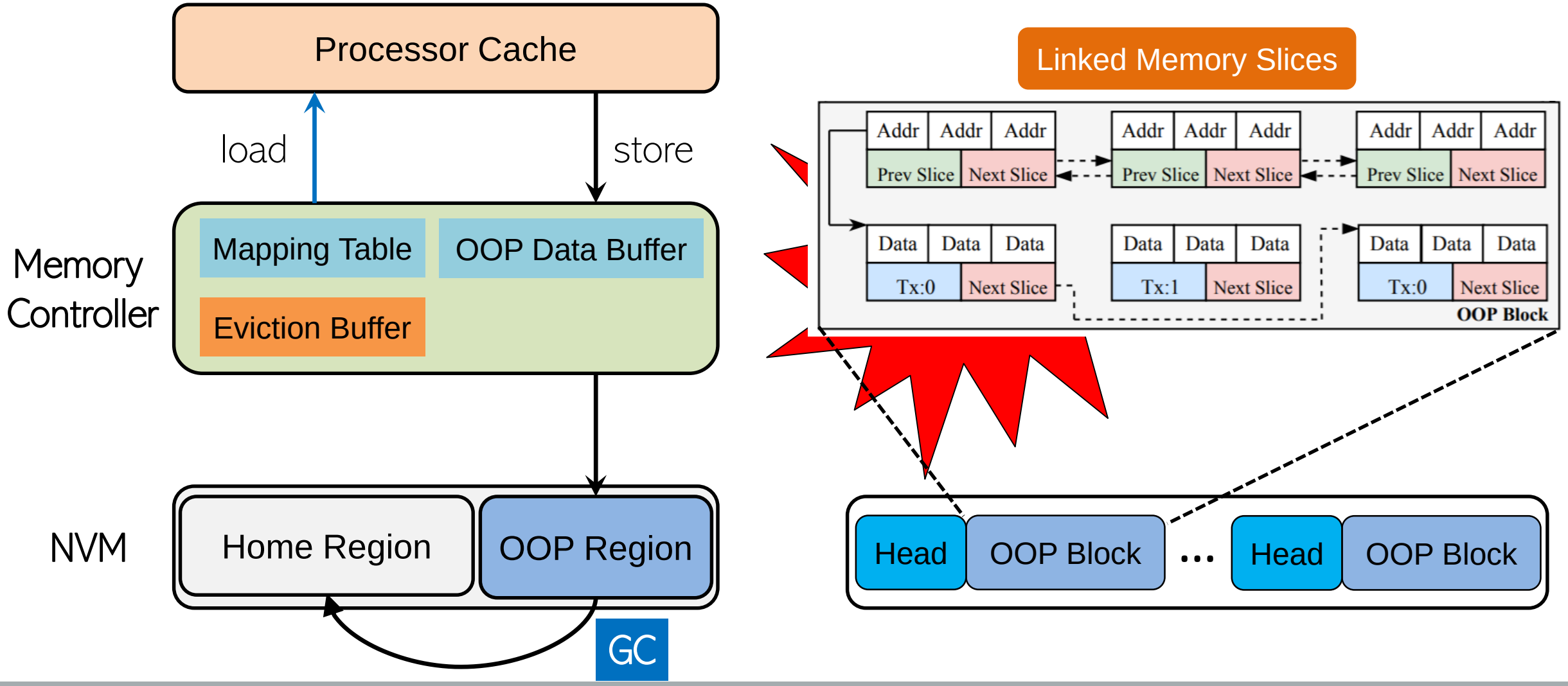
Data Packing in the Memory Controller for Improved Performance



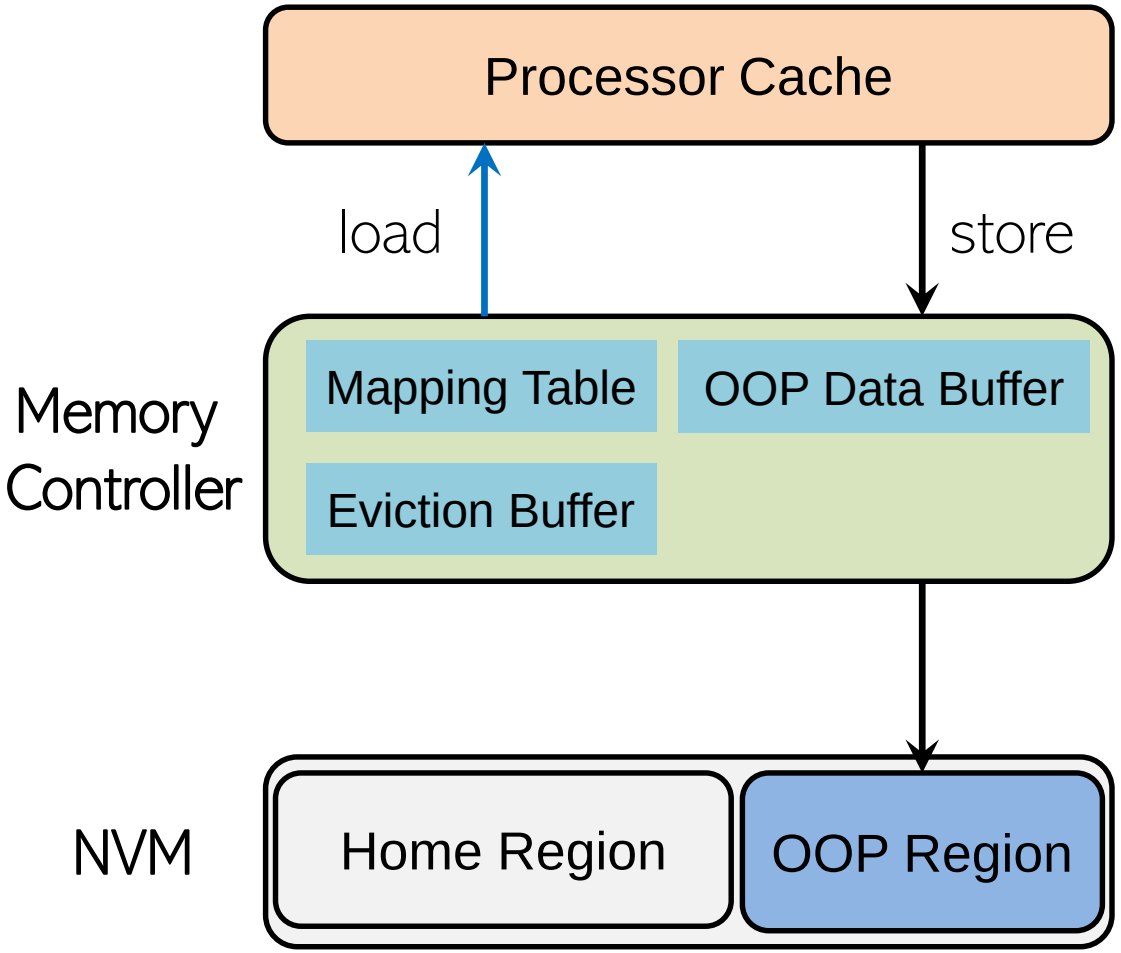
Ensuring Persistence Ordering in the Memory Controller

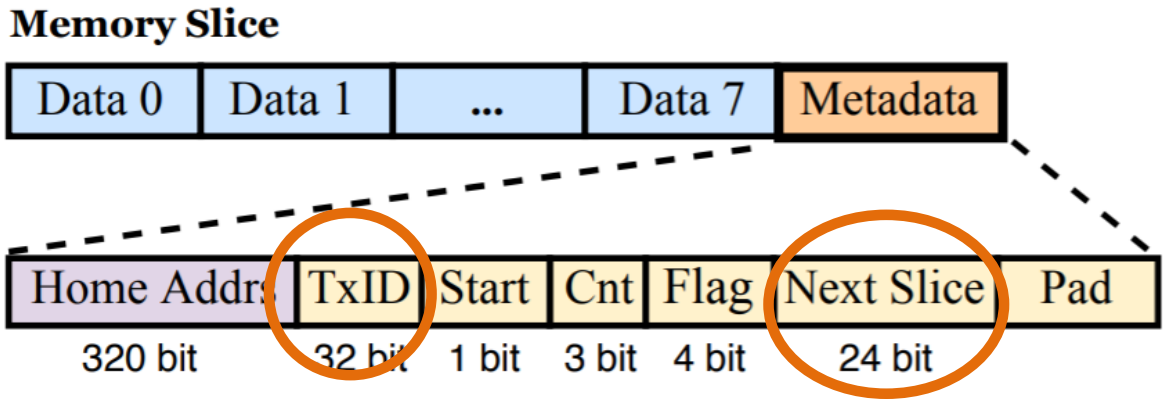


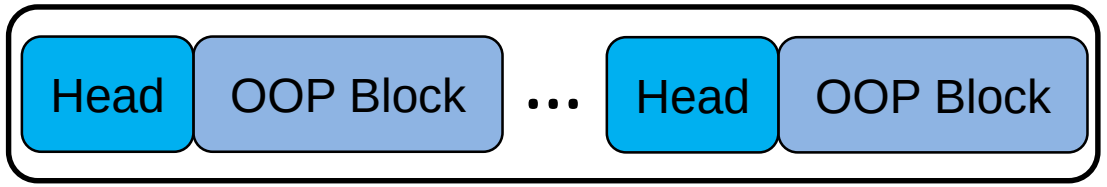
Efficient Garbage Collection for Improved Memory Utilization



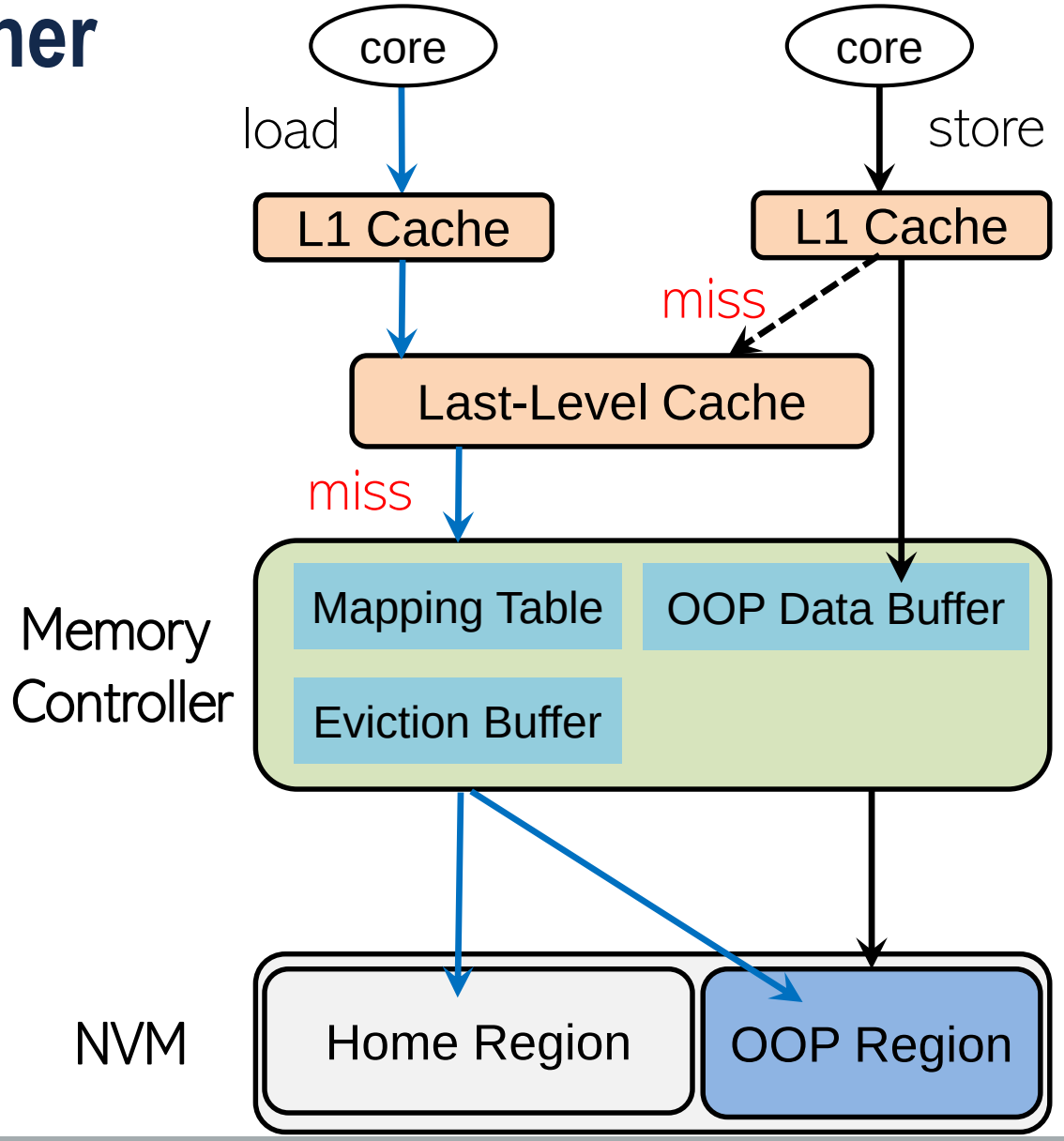
Handling Crash Consistency Upon Failures







Put It All Together



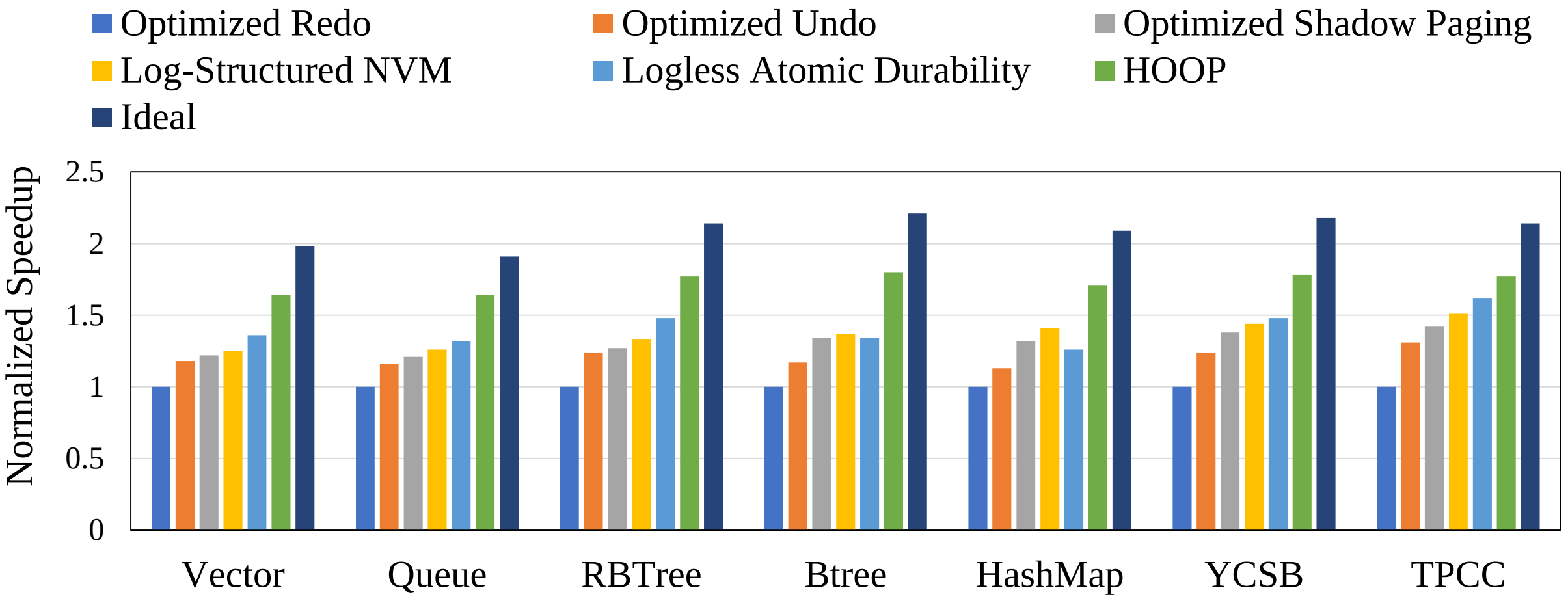
HOOP Implementation

Processor Simulator	McSimA+: OoO cores, 2.5GHz, 32KB L1, 256KB L2, 2MB LLC
NVM Simulator	Read/Write = 50/150ns, 512GB

Evaluation Benchmarks

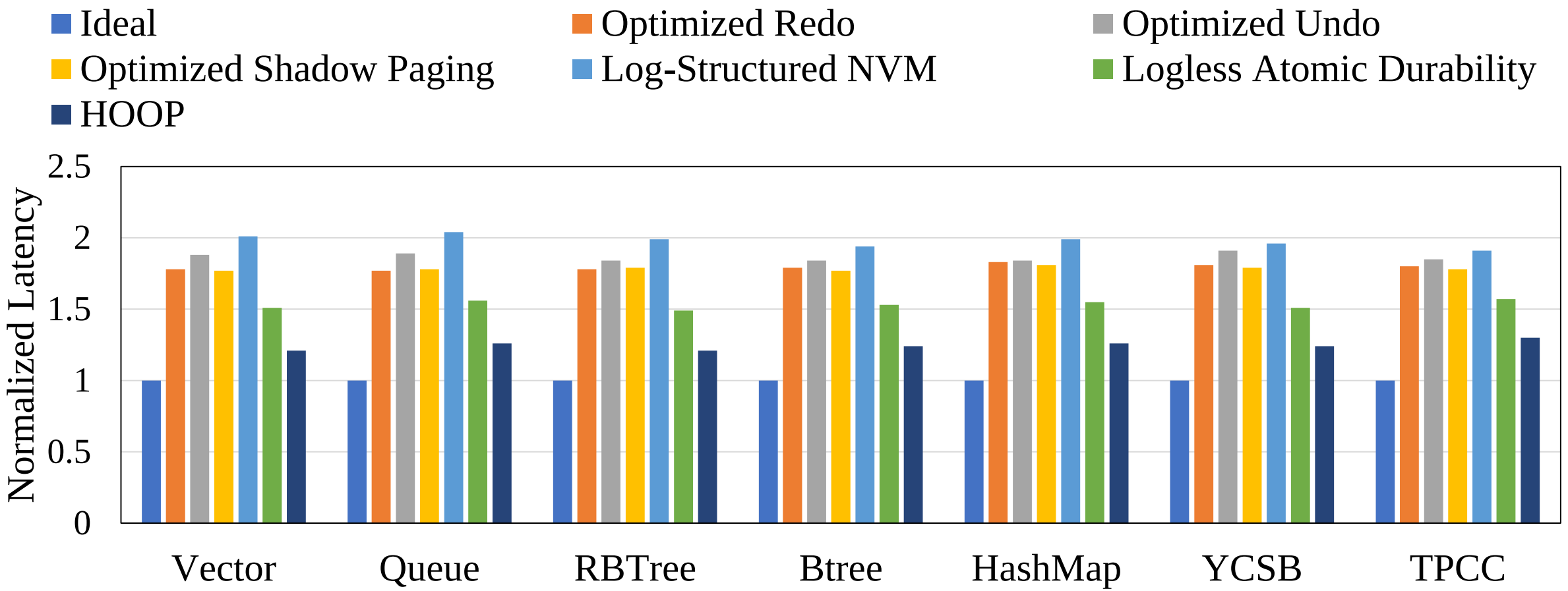
Synthetic Workloads	Vector, HashMap, Queue, RB-Tree, B- Tree
Real-world Workloads	YCSB, TPCC

Improving Transaction Throughput with HOOP



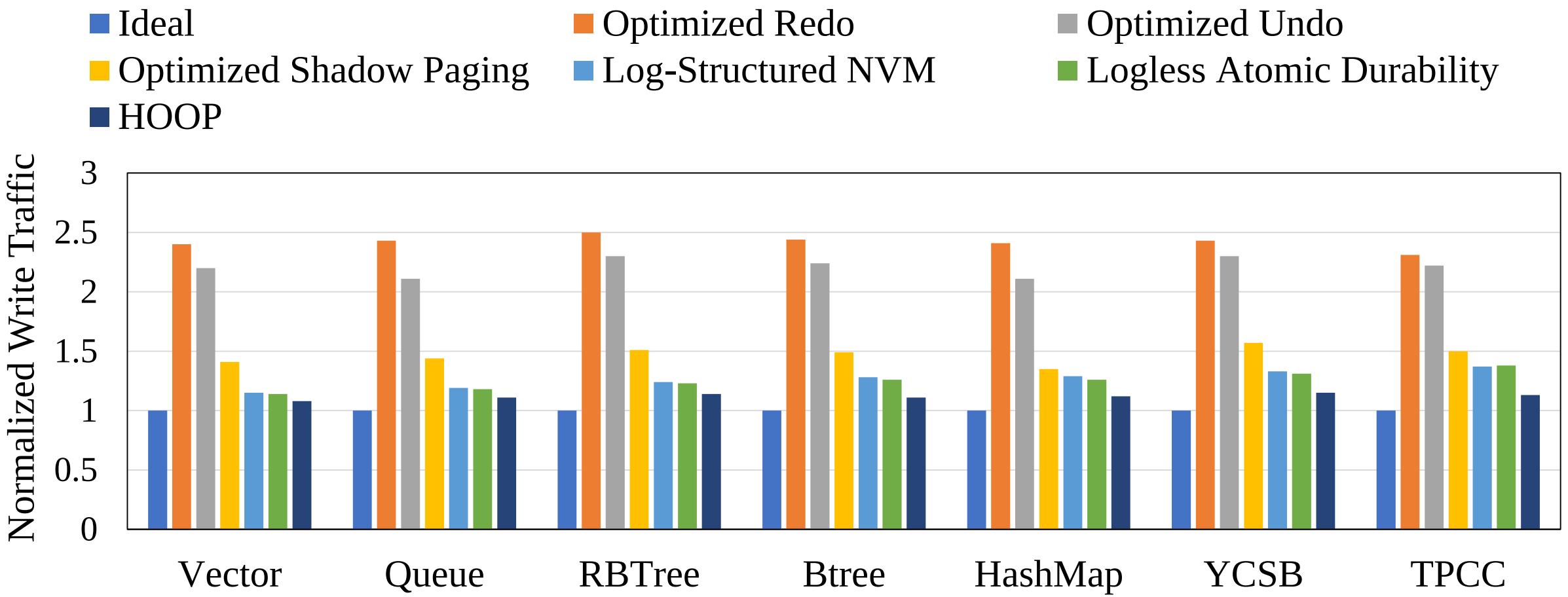
HOOP is close to the performance of a system without any persistence enforcement.

Reducing Critical-Path Latency with HOOP



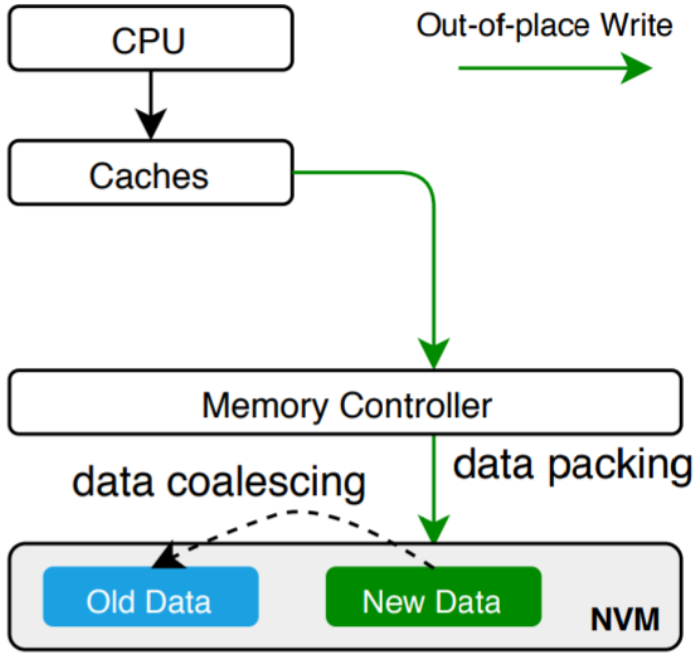
HOOP achieves the lowest latency, compared to state-of-the-art approaches.

Reducing Write Traffic with HOOP



HOOP reduces write traffic by up to 2.1x, compared to logging approaches.

HOOP Summary



1.7x Performance Speedup for Data-Intensive Apps

2.1x Reduction of Write Amplification

Thanks!

Miao Cai Chance Coats Jian Huang

Systems Platform Research Group

University of Illinois at Urbana-Champaign
Electrical & Computer Engineering